REMARKS

Responsive to the Office Action mailed on March 22, 2005 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the reference signs 203d and 203e mentioned in the description. Claims 1-3 stand rejected under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Claims 1-4 stand rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al (US Patent No. 6,656,796).

In this paper, the figures are amended to overcome the objections, as described in further detail below. Claims 1 and 4 are amended. Namely, claim 1 is amended to recite the limitation "a gate dielectric layer interposed between the semiconductor substrate and the conductive base so as to directly contact with the first bottom portion." Claim 4 is amended to recite "the protruding poly layer on the base poly layer." Support for the amendments can be found on page 7 and in Figs. 2g and 2f of the application. Typographical errors in claims 1 and 4 are also corrected. The summary is amended to correspond to the amended claims. Thus, after entry of this amendment, claims 1-4 remain in the application.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the reference signs 203d and 203e mentioned in the description. Fig. 2g has been amended to include reference signs 203d and 203e, as described in the specification. Applicant submits that the objection to the drawings is thereby overcome.

Rejections Under 35 U.S.C. 112

Claims 1-3 stand rejected under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. In this paper, the limitation "and the first bottom portion contacts to the semiconductor substrate" in original claim 1 is canceled to comply with 35 U.S.C 112. Applicant respectfully asserts that the rejection is thereby overcome.

Rejections Under 35 U.S.C. 102

Claims 1-4 stand rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al. To the extent that the grounds of the rejections may be applied to the claims now pending in this application, they are respectfully traversed.

Claim 1

As amended, claim 1 recites a floating gate formed on the surface of a semiconductor substrate, comprising a conductive base having a first top portion and a first bottom portion, wherein an edge of the first top portion is a first tip; ***a gate dielectric layer interposed between the semiconductor substrate and the conductive base so as to directly contact with the first bottom portion***; ***a conductive protruding layer protruding from the conductive base, and the conductive protruding layer has a flat top***, wherein the conductive protruding layer has a second top portion and a second bottom portion, an edge of the second top portion is a second tip, the second bottom portion is connected to the first top portion, ***the conductive protruding layer has two concave sidewalls***; and wherein a multiple tip floating gate is composed of the conductive base and the conductive protruding layer.

To anticipate a claim, a reference must teach every element of the claim. In this regard, the Federal Circuit has held:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In claim 1, a stacked structure is described, with the conductive base sandwiched between the gate dielectric layer and the conductive protruding layer. Namely, the bottom portion of the conductive base contacts the gate dielectric layer, and the bottom portion of the conductive protruding layer is connected to the top portion of the conductive base. Applicant notes that it is the conductive protruding layer, i.e., the top layer of the stack, that has a flat top and concave sidewalls, not the middle layer.

Chan et al disclose a split gate field effect transistor (FET) device. The floating gate electrode (14a) is a multiple tip floating gate composed of a conductive base and a conductive protruding layer. See Fig. 6.

The conductive base has a first bottom portion and a first top portion. The first bottom portion directly contacts with the gate dielectric layer (12a). The first top portion has a pair of pointed tips 21c and 21d. See column 8, lines 23-33 and Fig. 6 of Chan et al.

The conductive protruding portion has a second bottom portion and a second top portion. The second bottom portion contacts the first top portion of the conductive base. The second top portion has a pair of pointed tips 21a and 21b. See column 8, lines 23-33 and Fig. 6 of Chan et al.

As clearly shown in Fig. 6, Chan et al fail to disclose that the conductive protruding portion has a flat top. On the contrary, the conductive protruding portion has an arc-shaped top or a concave top. See Fig. 6, between tips 21a and 21b.

Furthermore, Chan et al fail to disclose a conductive protruding portion having two concave sidewalls. On the contrary, the conductive protruding portion in Chan et al has straight sidewalls. See Fig. 6, between tips 21a and 21c, and between tips 21b ad 21d.

As Chan et al do not teach or suggest all of the limitations recited in claim 1 of the present application, it is applicant's belief that this claim is allowable over the cited reference. Insofar as claims 2-3 depend from claim 1, these claims are also allowable.

Claim 4

As amended, claim 4 recites a floating gate formed on the surface of a semiconductor substrate, with a gate dielectric layer formed between the floating gate and the semiconductor substrate, comprising a base poly layer having a first top portion and a first bottom portion, wherein an edge of the first top portion is a first tip, and ***the first bottom portion contacts to the gate dielectric layer***; and ***a protruding poly layer on the base poly layer***, wherein ***the protruding poly layer has a flat top***, a second top portion and a second bottom portion, an edge of the second top portion is a second tip, the second bottom portion contacts the first top portion, ***the protruding poly layer has two concave sidewalls***, wherein a multiple tip floating gate is composed of the base poly layer and the protruding poly layer.

Thus, in claim 4, a stacked structure is described, with the base poly layer sandwiched between the gate dielectric layer and the protruding poly layer. Namely, the bottom portion of the base poly layer contacts the gate dielectric layer. The bottom portion of the protruding poly layer contacts the top portion of the base poly layer. Applicant notes that it is the protruding poly layer, i.e., the top layer of the stack, that has a flat top and concave sidewalls, not the middle layer.

As noted above, Chan et al disclose a split gate field effect transistor (FET) device. The floating gate electrode (14a) is a multiple tip floating gate composed of a base layer and a protruding layer, where the conductive protruding layer is on the base layer. See Fig. 6.

The base layer has a first bottom portion and a first top portion. The first top portion as a pair of pointed tips 21c and 21d. The first bottom portion contacts the gate dielectric layer 12a. See column 8, lines 23-33 and Fig. 6 of Chan et al.

The protruding layer is on the base layer and has a second bottom portion and a second top portion. The second bottom portion contacts the first top portion of the base layer. The second top portion has a pair of pointed tips 21a and 21b. See column 8, lines 23-33 and Fig. 6 of Chan et al.

As clearly shown in Fig. 6, Chan et al fail to disclose that the protruding layer has a flat top. On the contrary, the protruding layer has an arc-shaped top or a concave top. See Fig. 6, between tips 21a and 21b.

Furthermore, Chan et al fail to disclose a protruding layer having two concave sidewalls. On the contrary, the protruding layer in Chan et al has straight sidewalls. See Fig. 6, between tips 21a and 21c, and between tips 21b ad 21d.

As Chan et al do not teach or suggest all of the limitations recited in claim 4 of the present application, it is applicant's belief that this claim is allowable over the cited reference.

Prior Art in Earlier Application

This application is a divisional application of U.S. Patent Application Serial No. 10/436,800, filed on May 13, 2003. The Examiner is reminded to consider the prior art cited in the parent application. MPEP 609 and 2001.06(b).

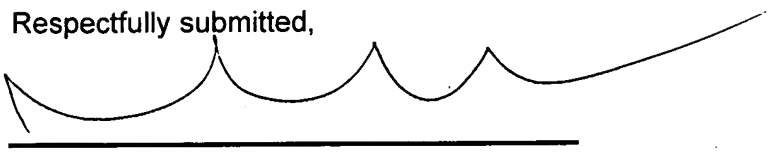
Foreign Priority Claim

Acknowledgment of Applicant's claim to foreign priority under 35 USC 119(a)-(d) or (f) and receipt of the certified copies of the priority document(s) in the parent application is respectfully requested.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

Respectfully submitted,



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AMENDMENTS TO THE DRAWINGS

The attached one (1) sheet of drawings replaces the original sheet for Fig. 2g and includes changes to Fig. 2g.

Attachment: Replacement Sheets (1)